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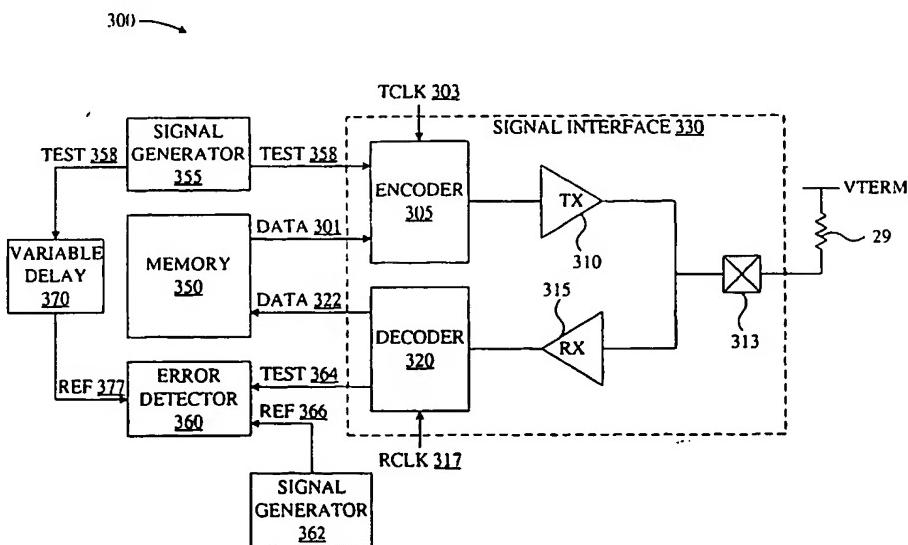
(57) Abstract: Error detection mechanisms for signal interfaces are disclosed, including built-in self-test (BIST) mechanisms (300) for testing multilevel signal interfaces (330). The error detection mechanisms may be provided in an integrated circuit (IC) chip that contains at least one of the signal interfaces or may be coupled to the interfaces on a printed circuit board (PCB). BIST mechanisms may include, for example, test signal generators (355, 362) and mechanisms (360) for determining whether the test signals generated are accurately transmitted and received by the interface. The BIST mechanisms may check a single input/output interface (330, 502), a group of interfaces (410, 420, 430) or may operate with a master device that tests a plurality of interfaces (616, 617). The error detection mechanisms may be particularly advantageous for testing memory circuits (611, 612, 613) designed to communicate according to multi-PAM signals over printed circuit boards (601).

BUILT-IN SELF-TESTING OF MULTILEVEL SIGNAL INTERFACES

BACKGROUND OF THE INVENTION

5   The present invention relates to multilevel digital signaling, and in particular to mechanisms to test for errors that may occur in a multilevel, multi-line signaling system.

The use of multiple signal levels instead of binary signal levels is a known technique for increasing the data rate of a digital signaling system, without necessarily

10   increasing the signal frequency of the system. Such multilevel signaling is sometimes known as multiple pulse amplitude modulation or multi-PAM, and has been implemented with radio or other long-distance wireless signaling systems.

Other long-distance uses for multi-PAM signaling include computer or telecommunication systems that employ Gigabit Ethernet over optical fiber (IEEE

15   802.3z) and over copper wires (IEEE 802.3ab), which use three and five signal levels, respectively, spaced symmetrically about and including ground.

Multi-PAM has not traditionally been used for communication between devices in close proximity or belonging to the same system, such as those connected to the same integrated circuit (IC) or printed circuit board (PCB). One reason for this

20   may be that within such a system the characteristics of transmission lines, such as buses or signal lines, over which signals travel are tightly controlled, so that increases in data rate may be achieved by simply increasing data frequency. At higher frequencies, however, receiving devices may have a reduced ability to distinguish binary signals, so that dividing signals into smaller levels for multi-PAM is

25   problematic. Multi-PAM may also be more difficult to implement in multi-drop bus systems (i.e., buses shared by multiple processing mechanisms), since the lower signal-to-noise ratio for such systems sometimes results in bit errors even for binary signals.

Testing of a multi-PAM device is also problematic, since test apparatuses are

30   typically designed for testing binary signals. Thus, in addition to the complexities of designing a multi-PAM device, conventional ways of testing a multi-PAM device to ensure that the device operates free of errors may be lacking.

SUMMARY

Error detection mechanisms for signal interfaces are disclosed, including built-in self-test (BIST) mechanisms for testing multilevel signal interfaces. The error detection mechanisms may be provided in an integrated circuit (IC) chip that contains at least one of the signal interfaces, or may be coupled to the interfaces on a printed circuit board (PCB). BIST mechanisms may include, for example, test signal generators and mechanisms for determining whether the test signals generated are accurately transmitted and received by the interface. The BIST mechanisms may check a single input/output interface, a group of interfaces or may operate with a master device that tests a plurality of slave device interfaces. The error detection mechanisms may be particularly advantageous for testing memory circuits designed to communicate according to multi-PAM signals over printed circuit boards.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a diagram of a multilevel signaling system having four logical states corresponding to four voltage ranges.

FIG. 2 is a diagram of a representative multilevel signaling device that may be used to create the voltage levels of FIG. 1.

FIG. 3 is a diagram of a differential 4-PAM signaling system.

FIG. 4A is a diagram of a pair of encoders translating binary signals into multiplexed control signals for the multilevel signaling device of FIG. 2.

FIG. 4B is a diagram of one of the encoders of FIG. 4A that encodes MSB even and LSB even signals into control signals.

FIG. 5A is a diagram of a receiver and decoder that receives the multilevel signals sent by the signaling device of FIG. 2 and decodes the signals into binary MSB even and LSB even components.

FIG. 5B is a diagram of the receiver and decoder of FIG. 5A along with another receiver and decoder that receive the multilevel signals sent by the signaling device of FIG. 2 and decode the signals into binary MSB and LSB even and odd components.

FIG. 6 is a diagram of a device including a multilevel signal interface coupled to a memory, sequence generators and an error detector.

FIG. 7 is a diagram of a system including a multilevel signal interface having a plurality of interface units that are connectable in series for testing.

FIG. 8 is a diagram of a system including a signal interface grouped into plural bytes of multilevel signal interface units and a byte of binary signal interface units, with each of the multilevel signal interface units in a first byte being connectable to a corresponding multilevel signal interface unit in a second byte for testing.

FIG. 9A is a diagram of a set of four pseudo-random bit sequence generators that can generate signals for testing the system of FIG. 8.

FIG. 9B is a diagram of a single pseudo-random bit sequence generator that can generate a set of four signals for testing the system of FIG. 8.

FIG. 10 is a functional block diagram of a system including plural devices and a controller each having signal interface units that are connected to a bus, with the controller serving as a master and the devices acting as slaves for testing.

FIG. 11 is a perspective view of the system of FIG. 10 affixed to a printed circuit board (PCB) by being removably inserted into the connectors such as slots.

FIG. 12 is a perspective view of the system of FIG. 10 affixed to a PCB without connectors.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 shows a multilevel signal system having four logical states corresponding to four distinct voltage levels, VOUT0, VOUT1, VOUT2 and VOUT3. The voltage levels in this example are all positive relative to ground, and range as high as VTERM. VOUT0 is defined to be above VREFH, VOUT1 is defined to be between VREFM and VREFH, VOUT2 is defined to be between VREFL and VREFM, and VOUT3 is defined to be less than VREFL. VOUT0 corresponds to logical state 00, VOUT1 corresponds to logical state 01, VOUT2 corresponds to logical state 11, and VOUT3 corresponds to logical state 10. An example of the 4-PAM system described above has been implemented for a memory system interface having VOUT0=1.80V, VOUT1=1.533V, VOUT2=1.266V and VOUT3=1.00V. Although four logical states are illustrated in this example, a multilevel signal system may have more or less logical states, with at least two reference levels serving as boundaries between the states.

A first bit of each logical state is termed the most significant bit (MSB) and a second bit of each logical state is termed the least significant bit (LSB). Each logical state may be termed a symbol, since it provides information regarding more than one bit. Data may be transmitted and read at both rising and falling edge of a clock cycle,

3

so that each bit signal and each dual-bit signal has a duration of one-half the clock cycle. The logical states are arranged in a Gray coded order, so that an erroneous reading of an adjacent logic state produces an error in only one of the bits. Another characteristic of this logical 4-PAM arrangement is that setting the LSB equal to zero

5   for all states results in a 2-PAM scheme. Alternatively, the logical states can be arranged in numerical (00, 01, 10, 11) or other order.

In one embodiment the communication system is employed for a memory bus that may for instance include random access memory (RAM), like that disclosed in U.S. Patent Number 5,243,703 to Farmwald et al., which is incorporated herein by

10   reference. The multi-PAM communication and testing techniques disclosed herein may also be used for other contained systems, such as for communication between processors of a multiprocessor apparatus, or between a processor and a peripheral device, such as a disk drive controller or network interface card over an input/output bus.

15   FIG. 2 shows a representation of a communication system that may be used to create the voltage levels of FIG. 1. An output driver 20 drives signals to output pad 18 and over a signal pathway such as transmission line 16, which may for example be a memory bus or other interconnection between devices affixed to a circuit board, to be received at pad 25. Transmission line 16 has a characteristic impedance Z_0 27 that

20   is substantially matched with a terminating resistor 29 to minimize reflections.

Output driver 20 includes first 21, second 22 and third 23 transistor current sources, which together produce a current I when all are active, pulling the voltage at pad 25 down from VTERM by $I \cdot Z_0$, signaling logical state 10 under the Gray code system. Control signal input through lines C1, C2 and C3 switch respective current

25   sources 21, 22 and 23 on and off. To produce voltage VOUT0=VTERM, signaling logical state 00, current sources 21, 22 and 23 are all turned off. To produce voltage VOUT1=VTERM-(1/3)$I \cdot Z_0$, signaling logical state 01, one of the current sources is turned on, and to produce voltage VOUT2=VTERM-(2/3)$I \cdot Z_0$, two of the current sources are turned on. The logical level 00 is chosen to have zero current flow to

30   reduce power consumption for the situation in which much of the data transmitted has a MSB and LSB of zero. The reference levels are set halfway between the signal levels, so that VREFH=VTERM-(1/6) $I \cdot Z_0$, VREFM=VTERM-(1/2) $I \cdot Z_0$ and VREFL=VTERM(5/6) $I \cdot Z_0$.

FIG. 3 shows an example of a differential 4-PAM signaling system where data is encoded on two wires or other transmission media and a symbol value is determined by the voltage difference as measured by a receiver. The use of differential signaling can provide increased immunity to noise and crosstalk. A

5   voltage V1 on one of the wires varies over time between four voltage levels, as shown with solid line 50, while a voltage V2 on the other wire also varies between the four voltage levels but in a complementary fashion, as shown with broken line 55. Voltage differences VDIFF between voltages V1 and V2 for times T1, T2, T3 and T4 are listed above the signals in arbitrary units as +3, +1, -1 and –3, respectively. The MSB

10   and LSB symbols corresponding to the voltage differences are listed above the signals in Gray coded sequence.

Another example of a multilevel signaling apparatus and method is disclosed in U.S. Patent Number 6,005,895 to Perino et al., which is also incorporated herein by reference. This and other types of multilevel signal interfaces may also be tested in

15   accordance with the present invention. Also incorporated by reference herein is a U.S. Patent application that discloses other means for testing multilevel signal interfaces, entitled "Multilevel Signal Interface Testing with Binary Test Apparatus by Emulation of Multilevel Signals," filed on the same date as the present application by inventors Werner, Zerbe, Stonecypher, Liaw and Chang.

20   FIG. 4A shows an embodiment for which data is transmitted and read at both rising and falling clock edges, using a pair of substantially identical encoders 100 and 120 translating MSB and LSB odd and even signals into the control signals on lines C1, C2 and C3 for output driver 20. MSB even and LSB even signals on lines MSBE and LSBE are input to encoder 100, which outputs thermometer code signals on lines

25   C1E, C2E and C3E. Similarly, and MSB odd and LSB odd signals on lines MSBO and LSBO are input to encoder 120, which outputs thermometer code signals on lines C1O, C2O and C3O. Lines C1E and C1O input to multiplexer 106, lines C2E and C2O input to multiplexer 102, and lines C3E and C3O input to multiplexer 112. Multiplexers 102, 106 and 112 select the odd or even signals according to a clock

30   select signal on select line 118, outputting the thermometer code control signals on lines C1, C2 and C3.

Encoder 100 is shown in more detail in FIG. 4B. MSBE is connected to line C2E. MSBE is also input to an OR gate 104 that has LSBE as its other input, with the output of OR gate 104 connected to line C1E. Signals on line LSBE pass through

inverter 108, with the inverted signals on line LSBE_B input to AND gate 110. AND
gate 110 receives as its other input line MSBE, with its output connected to line C3E
providing a third control signal.

Table 1 illustrates the correspondence between MSB and LSB signals and the
control signals on lines C1, C2 and C3 that translate binary signals into 4-PAM
signals.

<div align="center">Table 1</div>

MSB	LSB	C1	C2	C3
0	0	0	0	0
0	1	1	0	0
1	1	1	1	0
1	0	1	1	1

For example, when MSB=0 and LSB=0, all the control signals are off. When
MSB=0 and LSB=1, the OR gate 104 outputs on, so that the control signal on line C1
is on, but control signals on lines C2 and C3 are still off. When both MSB=1 and
LSB=1, control signals on lines C1 and C2 are on, but due to inverted LSB signals
input to AND gates such as AND gate 110, the control signal on line C3 is off.
When MSB=1 and LSB=0, control signals on all the lines C1, C2 and C3 are turned
on. In this fashion the MSB and LSB may be combined as Gray code and translated
to thermometer code control signals on lines C1, C2 and C3 that control the current
sources to drive 4-PAM signals.

FIG. 5A shows one possible embodiment of a receiver 200 that may be used to
receive the multilevel signals sent by drivers such as those described above, and
decode the signals into MSBE and LSBE components. As mentioned above, the data
may be transmitted at twice the clock frequency, and a substantially identical receiver
240 is shown in FIG. 5B, with receivers 200 and 240 reading even and odd data,
respectively.

An MSBE receiver 202 of the 4-PAM receiver 200 in this example receives
and decodes a 4-PAM input signal VIN by determining whether the signal VIN is
greater or less than VREFM. In the MSBE receiver 202, a latching comparator 204
compares the value of the voltage of the received input signal VIN to the reference
voltage VREFM and latches the value of the result of the comparison B in response to

a receive clock signal RCLOCK. Although this embodiment discloses data sampling at both rising and falling clock edges, data may alternatively be sampled at only the rising clock edges or only the falling clock edges.

In an LSBE receiver 208, two latching comparators 210 and 214 compare the value of the voltage of the received input signal VIN to the reference voltages VREFH and VREFL, and latch the value of the result of the comparison A and C, respectively, in response to the receive clock signal. To decode the LSBE, the signals from the comparator outputs B, A, and C are then passed through combinational logic 220. The latching comparators 204, 210 and 214 may be implemented as integrating receivers to reduce the sensitivity of the output signals to noise. This can be accomplished by integrating the difference between the received signal, Vin, and the three respective reference voltages over most or all of the bit cycle, and then latching the integrated results as the outputs A, B and C. Related disclosure of a multi-PAM signaling system can be found in U.S. Patent Application Serial Number 09/478,916, entitled "Low Latency Multi-Level Communication Interface," filed on January 6, 2000, which is incorporated by reference herein.

FIG. 6 shows a functional block diagram of one type of device 300 including a multilevel signal interface 330 coupled to an optional memory 350, both of which may be tested in accordance with the present invention. Memory 350 may store data in binary or other form using semiconductor, magnetic, optical, ferroelectric or other known means for storage. Data signals 301 from memory 350 are clocked with transmit clock signals 303 and encoded at encoder 305, which provides control signals that drive output driver or transmitter 310. Multilevel signals are transmitted by transmitter 310 to input/output pin 313, which affords communication between device 300 and other devices, not shown in this figure.

Encoder 305 and transmitter 310, which together function as a transmit mechanism, may be similar to encoder 100 and output driver 20 described previously, and input/output pin 313 may be similar to pads 18 or 25 described above, for example. Also coupled to input/output pin 313 is receiver 315, which is adapted to detect multilevel signals from pin 313. The output of receiver 315 is sampled with receive clock signals 317 and decoded into binary signals at decoder 320 to be communicated as data 322 for storage in memory 350. Receiver 315 and decoder 320 may be similar to receive mechanism 200 described previously.

To use device 300 for data storage, multilevel signals may be received at I/O

pin 313 from a device external to this figure, such as a transmitter or processor

connected to pin 313 by a signal pathway such as a conductive line. Those multilevel

signals may be detected by receiver 315, translated to binary signals by decoder 320,

5   and sent as data 322 for storage in memory 350. To read information from memory

350, data 301 is sent to encoder 305, which causes transmitter 310 to send multilevel

signals to I/O pin 313 for transmission to the external device.

In addition to the data storage mechanisms described above, device 300

includes a signal generator 355 that creates test signals 358 for testing signal interface

10   330. Signal generator 355 may, for example, include a linear feedback shift register

(LFSR) that generates a predictable series of test signals 358, or may include another

known pseudo-random bit sequence (PRBS) generator. As an alternative example,

signal generator 355 may be programmed to output a known sequence of signals

designed to test worst case transitions of the interface 330 or memory 350.

15   In a test mode, test signals 358 from signal generator 355 may be fed to

encoder 305, which causes multilevel signals to be sent by transmitter 310. In

contrast with conventional operation, receiver 315 is enabled to detect the multilevel

signals and provide them to decoder 320. Decoder 320 translates the multilevel

signals to binary test signals 364 that are output to an error detector 360, which

20   determines whether test signals 358 have been accurately transmitted by signal

interface 330. Error detector 360 may include a comparison mechanism such as one

or more comparitors or other logic elements.

To make this determination, device 300 may include a second signal generator

362 that creates a series of reference signals 366 for comparison with test signals 364.

25   Signal generator 362 may be substantially identical to signal generator 355, e.g., both

may be a LFSR having an identical number of bits. To synchronize signal generator

362 with signal generator 355 in this case, an initial set of test signals 364 may be

loaded into the shift register of signal generator 362. Alternatively, signal generator

355 may be connected to a variable delay element 370 that delays test signals 358 by

30   an amount substantially equal to the delay of signal interface 330, to provide reference

signals 377 to error detector 360, for comparison with test signals 364. Variable delay

element 370 may include a plurality of essentially static delay elements, such as flip-

flops, as well as a tunable delay element, to form a kind of phase-locked loop (PLL)

or delay-locked loop (DLL).

Delay element 370 may also be offset from its ideal timing so that the timing margin may be determined for either transmitting or receiving data. Likewise, each of the reference voltages in Fig 4A may be varied to determined voltage margins for multi-PAM data.

5   FIG. 7 illustrates a system 400 including a multilevel signal interface 404 having a plurality of signal interface units (410, 420, 430) that are connectable in series for testing, although during operation the signal interface units are arranged to communicate separately or in parallel. That is, during testing the signal interface units are 410, 420 and 430 are enabled for self-testing as described above with

10   reference to FIG. 6, and adjacent signal interface units are also connected to forward test signals from one signal interface unit to the next. During operation, however, signal interface units 410, 420 and 430 separately or in parallel communicate with outside entities via respective I/O pins 418, 428 and 438.

A first signal interface unit 410 includes a first transmit mechanism 414, a first

15   receive mechanism 416 and a first I/O pin 418. A second signal interface unit 420, which includes a second transmit mechanism 424, a second receive mechanism 426 and a second I/O pin 428, is coupled to first signal interface unit 410 via an optional first multiplexer-demultiplexer 412. First multiplexer-demultiplexer 412 can select to bypass second signal interface unit 420 by connecting instead to an optional second

20   multiplexer-demultiplexer 422. Second multiplexer-demultiplexer 412 selects whether second signal interface unit 420 communicates with or bypass a third signal interface unit, not shown.

In this manner N signal interface units may be daisy-chained for testing, with an Nth signal interface unit 430 including an Nth transmit mechanism 434, an Nth

25   receive mechanism 436 and an Nth I/O pin 438, the Nth signal interface unit 430 coupled to the other signal interface units with another multiplexer-demultiplexer, not shown. Each transmit mechanism and each receive mechanism times the signals with clock signals, which may be sent from a master clock generator, not shown in this figure. A first signal generator 440 is coupled to the first signal interface unit 410 via

30   an optional demultiplexer 408, which can be switched to instead bypass first signal interface unit 410. An error detector 444 is coupled to the Nth interface unit 430 and a second signal generator 448 is coupled to the error detector 444.

To test the signal interface 404, signal generator 440 sends a test signal or series of test signals to first transmit mechanism 414, which in turn sends test signals

to first receive mechanism 416, in a fashion similar to that described above with regard to FIG. 6. Multiplexer-demultiplexer 412 can be set to send the signals from first receive mechanism 416 to second transmit mechanism 424, which in turn drives signals that are detected by second receive mechanism 426. The signals are thus

5   forwarded to Nth receiver 436, which outputs signals that are detected by error detector 444. An optional multiplexer 432 can select instead to provide signals to error detector 444 that bypass Nth interface unit 430.

Error detector 444 also receives signals from a second signal generator 448, which are compared with the signals from Nth receiver 436 that are detected by error

10   detector 444. The signals from second signal generator 448 are designed to be substantially identical to the test signals output by first signal generator 440 but delayed by a time period substantially equal to the delay encountered in passing through the series of interface units of the signal interface 404. If the signal or series of signals received by error detector 444 from Nth receiver 436 do not match the

15   signal or series of signals received by error detector 444 from second signal generator 448, then error detector 444 outputs an error signal.

A system such as that shown in FIG. 7 has an advantage of being able to test plural interface units with only one or two signal generators. Such testing of multiple interface units can save time for the situation in which errors are not common. In one

20   exemplary embodiment, system 400 may include eight or nine interface units, so that a byte of information may be communicated in parallel through I/O pins 418, 428 and 438 at any given time. For an IC that includes testing means along with a signal interface, such as that shown in FIG. 7, reducing the number of signal generators per interface unit reduces the chip real estate that is devoted to testing.

25   If an error is found in the signal interface 400, the multiplexers and demultiplexers, or similar logic circuits that select between two inputs and two outputs, can be set to test the individual interface units until the defective unit or units are identified. Alternatively, the individual interface units may be tested initially for errors, or a subset of the interface units may be tested, by appropriate settings of the

30   multiplexers and demultiplexers. In this manner the multiplexers and demultiplexers allow any subset of the N signal interface units to be tested.

FIG. 8 shows a system 500 including a multilevel signal interface 502 having multiple interface units arranged to facilitate communicating bytes of information. The interface units are grouped into two data communication bytes, A-BYTE 505 and

B-BYTE 511, which each include nine multilevel signal interface units in one embodiment, and a control or request byte R-BYTE 515, which includes eight binary signal interface units in this embodiment. The interface units in A-BYTE 505 and B-BYTE 511 may be similar to the multilevel interface units described above, each

5   interface unit having a mechanism for transmitting and receiving multilevel signals, with one of the interface units in both A-BYTE 505 and B-BYTE 511 used for parity signaling. A memory chip or controller, for example, may have one or more interfaces such as interface 502. Provided that termination and DC loading requirements are met, then A-BYTE 505 may be connected to a plurality of bytes

10   such as B-BYTE 511, and any two such bytes could test each other.

Each interface unit of A-BYTE 505 includes an I/O pin in a group of I/O pins labeled 520. Each interface unit of B-BYTE 511 and each interface unit in R-BYTE 515 also includes an I/O pin, disposed in a group of I/O pins labeled 522 and 525, respectively. Each interface unit in A-BYTE 505 is also coupled by a signal pathway

15   to a corresponding interface unit in B-BYTE 511, allowing the A-BYTE 505 to test the B-BYTE 511 and vice-versa.

A first PRBS generator or plurality of PRBS generators 530 may be coupled to the various interface units of A-BYTE 505, and a second PRBS generator or plurality of PRBS generators 533 may be coupled to the various interface units of B-BYTE

20   511. For the case in which first PRBS generator(s) 530 includes a plurality of different PRBS generators, each of those PRBS generators may be connectable to one or more of the interface units of A-BYTE 505. Similarly, for the case in which second PRBS generator 533 includes a plurality of different PRBS generators, each of those PRBS generators may be connectable to one or more of the interface units of B-

25   BYTE 511. An error detector 535 is coupled to first and second PRBS generator(s) 530 and 533.

To test the interface units in A-BYTE 505 and B-BYTE 511, first PRBS generator(s) 530 may output binary test signals to one or more of the interface units of A-BYTE 505, as shown by arrow 540. Each of the interface units of A-BYTE 505

30   that receives test signals from first PRBS generator(s) 530 sends multilevel signals to its corresponding interface unit in B-BYTE 511. The multilevel signals are detected by the corresponding interface unit in B-BYTE 511 and decoded to binary signals that are provided to error detector 535, as shown by arrow 544. Reference signals are sent from second PRBS generator(s) 533 to error detector 535, as shown by arrow 548, the

reference signals synchronized with the decoded signals. The decoded signals from B-BYTE 511 are compared at error detector 535 with the synchronized reference signals from second PRBS generator(s) 533. Error detector 535 outputs an error signal if the decoded and reference signals being compared do not match, indicating

5   that the transmit mechanism of A-BYTE 505 and/or the receive mechanism of B-BYTE 511 did not function properly.

Similarly, second PRBS generator(s) 533 may output binary test signals to one or more of the interface units of B-BYTE 511, as shown by arrow 550. Each of the interface units of B-BYTE 511 that receives test signals from second PRBS

10   generator(s) 533 sends multilevel signals to its corresponding interface unit in A-BYTE 505. The multilevel signals are detected by the corresponding interface unit in A-BYTE 505 and decoded to binary signals that are provided to error detector 535, as shown by arrow 552. Reference signals are sent from first PRBS generator(s) 530 to error detector 535, as shown by arrow 555, the reference signals synchronized with

15   the decoded signals. The decoded signals from A-BYTE 505 are compared at error detector 535 with the synchronized reference signals from first PRBS generator(s) 530. Error detector 535 outputs an error signal if the decoded and reference signals being compared do not match, indicating that the transmit mechanism of B-BYTE 511 and/or the receive mechanism of A-BYTE 505 did not function properly.

20   If the system 500 has less PRBS generators than interface units, the testing process may be repeated until all of the interface units have been tested. First PRBS generator(s) 530, or other PRBS generator(s), may be connected to R-Byte 515, and each of the interface units of R-Byte 515 of may be coupled to another of the interface units of R-Byte 515, allowing those interface units to test each other by comparing

25   signals transmitted and received at the error detector 535. Thus, testing of the multilevel signal interface can be accomplished by the means described above, without the need for additional test mechanisms to generate or detect multilevel signals.

FIG. 9A shows a set of four PRBS generators 560-563 that can generate

30   signals for testing the system of FIG. 8. The four PRBS generators 560-563 are identical but initialized or seeded with different bit settings, and may be used for example as PRBS generator(s) 530 of FIG. 8. A multiplexer, not shown in this figure, is provided to each of the bits to afford the choice of initializing the bit or running the PRBS. In this example, a first PRBS generator 560 is input as a MSBE signal to an

encoder such as encoder 305, while a second PRBS generator 561 is input as a LSBE signal to encoder 305, a third PRBS generator 562 is input as a MSBO signal to encoder 305, and a fourth PRBS generator 563 is input as a LSBO signal to encoder 305.

FIG. 9B shows a single PRBS generator 570 that can generate a set of four signals (MSBE, LSBO, LSBE and MMSBO) that can be input to an encoder, not shown in this figure, for testing the system of FIG. 8. PRBS generator 570 may be used for example as PRBS generator(s) 530 of FIG. 8. PRBS generator 570 has a first flip-flop 571, followed by four sets of four flip-flops 572-575, configured with exclusive-OR gates 582-585 as shown. Other PRBS generators known in the art may be used in place of those shown in FIG. 9A and FIG. 9B.

FIG. 10 shows a system 600 including a number of signal interfaces with built-in self-test mechanisms. The system 600 includes a control device CTRL 606 which may act as master to a number of other devices labeled A-CELL 611, B-CELL 612 and C-CELL 613. The control device CTRL 606 has first and second multilevel signal interfaces 616 and 617, as well as a binary or 2-PAM signal interface 618. Each of the signal interfaces may be a byte wide, similar to that described above with regard to FIG. 8. Likewise, A-CELL 611 has first and second multilevel signal interfaces 622 and 623, as well as a binary or 2-PAM signal interface 624, each of which may be a byte wide. Similarly, B-CELL 612 has first and second multilevel signal interfaces 632 and 633, as well as a binary signal interface 634, and C-CELL 613 has first and second multilevel signal interfaces 642 and 643, as well as a binary signal interface 644, each of which may be a byte wide.

Multilevel signal interfaces 616, 622, 632 and 642 are coupled to a first signal pathway such as bus 650, which may be a byte wide. Likewise, multilevel signal interfaces 617, 623, 633 and 643 are coupled to a second signal pathway such as bus 655, which may also be a byte wide. Similarly, binary signal interfaces 618, 624, 634 and 644 are coupled to a third signal pathway such as bus 660, which may also be a byte wide. Buses 650, 655 and 660 are terminated at VTERM with a matched impedance to reduce reflections.

Each of the devices 606 and 611-613 may have a test signal generator such as a PRBS generator and an error detector. In this case, receive mechanisms of devices 611-613 can be tested by sending signals from control device CTRL 606, and transmit mechanisms of devices 611-613 can be tested by sending signals sent to control

device CTRL 606. Alternatively, only control device CTRL 606 may have a PRBS generator and error detector, with devices 611-613 being tested by sending signals to receive mechanisms of devices 611-613, with corresponding transmit mechanisms of those devices 611-613 sending signals back to control device CTRL 606 for error

5   detection. Optionally, each of the signal interfaces 616-618, 622-624, 632-634 and 642-644 may be coupled to at least one test signal generator and error detector, and each interface unit of each of the signal interfaces 616-618, 622-624, 632-634 and 642-644 may be connected to a test signal generator. The choice of how many test mechanisms to employ along with each device may involve tradeoffs between the cost

10 of the test mechanisms, such as space required by the test mechanisms, and the ease and exactness of the testing.

As an example, to test the receive mechanisms of multilevel signal interface 622, multilevel signal interface 616 may be caused by a PRBS generator to send a series of test signals along bus 650 to interface 622, as shown by arrow 666.

15 Assuming that interface 622 has at least one PRBS detector, which may include a combination of PRBS generator and error detector, the PRBS detector can check whether the bus 650 and receive mechanism of signal interface 622 correctly received the signals. For the case in which a PRBS generator is provided for each interface unit of signal interface 616, and a PRBS detector is provided for each interface unit of

20 signal interface 622, the receive mechanisms of signal interface 622 and the bus 650 can also be tested for errors caused by cross-talk, for example along bus 650.

To test the transmit mechanisms of multilevel signal interface 642, that interface may be caused by a PRBS generator to send a series of test signals along bus 650 to multilevel signal interface 616, as shown by arrow 670. A PRBS detector

25 connected to interface 616 can check whether the bus 650 and transmit mechanism of signal interface 642 correctly sent the signals. For the case in which a PRBS generator is provided for each interface unit of signal interface 642, and a PRBS detector is provided for each interface unit of signal interface 616, the transmit mechanisms of signal interface 642 and the bus 650 can be tested for cross-talk

30 conditions as well.

To test multilevel signal interface 633, a series of test signals are sent by multilevel signal interface 617 along bus 655 to a receive mechanism of interface 634, as shown by arrow 672. Assuming that the receive mechanism of interface 633 is not coupled to a PRBS detector but instead to a memory and transmit mechanism of that

14

interface 633, the transmit mechanism can later send back a series of signals along
bus 655 to a receive mechanism of interface 617, as shown by arrow 677. A PRBS
detector connected to interface 617 can check whether the bus 655 and receive and
transmit mechanisms of signal interface 634 correctly relayed the signals over bus

5   655. For the case in which a PRBS generator is provided for each interface unit of
signal interface 617, the receive and transmit mechanisms of signal interface 633 and
the bus 655 can be tested for cross-talk conditions as well.

For example, control device CTRL 606 can transmit PRBS sequences through
interface 616 to interface 632, filling some or all of the addresses of a memory on B-

10   CELL 612. B-CELL 612 is then instructed to transmit all of the PRBS data from its
memory, the PRBS data being received by interface 616. Control device CTRL 606
can then check the data with a PRBS error detector.

Buses 650, 655 and 660 may be memory buses or other buses internal to an
apparatus such as a computer and may, for example, be affixed to a base such as a

15   PCB or may be part of an IC that is affixed to a base such as a wafer substrate.
Alternatively, buses 650, 655 and 660 may connect peripheral devices with a
computer, so that control device CTRL 606 may be representative of the computer
and A-CELL 611, B-CELL 612 and C-CELL 613 may be representative of peripheral
devices such as disk drives. As another example, buses 650, 655 and 660 may

20   represent networks connecting control device CTRL 606, A-CELL 611, B-CELL 612
and C-CELL 613. Further, although it may function as a master device, control
device CTRL 606 may be substantially identical to A-CELL 611, B-CELL 612 and/or
C-CELL 613. Control device CTRL 606 may also transmit master clock signals
along buses 650, 655 and 660 to synchronize various elements of A-CELL 611, B-

25   CELL 612 and C-CELL 613.

FIG. 11 shows an implementation in which system 600 comprises a high-
speed memory system, with control device CTRL 606 representing a controller and
A-CELL 611, B-CELL 612 and C-CELL 613 representing memory cells. The system
600 includes a base such as a PCB 601 (sometimes called a motherboard) to which a

30   memory controller 606, signaling paths 650, 655 and 660, and connectors 680, 684
and 688 are affixed. Memory modules 690, 694, and 698, each containing one or
more memory devices 611, 612 and 613, are affixed to the printed circuit board 601
by being removably inserted into the connectors 680, 684 and 688. Though not
shown in FIG. 11, the memory modules 690, 694, and 698 include traces to couple the

15

memory devices 611, 612 and 613 to the signaling paths 650, 655 and 660, and ultimately to the memory controller 606.

In the embodiment of FIG. 11FIG. 11, the signaling paths 650, 655 and 660 constitute multi-drop buses that are coupled to each memory module 690, 694, and

5   698. The individual memory devices of a given module may be coupled to the same set of signaling lines within signaling paths 650, 655 and 660, or each memory device of the module may be coupled to a respective subset of the signaling lines. In the latter case, two or more memory devices on a module may be accessed simultaneously to read or write a data value that is wider (i.e., contains more bits) than

10   the data interface of a single memory device. In an alternative embodiment (not shown), each of the memory modules may be coupled to the memory controller via a dedicated signaling path (i.e., a point-to-point connection rather than a multi-drop bus). In such an embodiment, each of the memory devices on the memory module may be coupled to a shared set of signaling lines of the dedicated path, or each

15   memory device may be coupled to respective subsets of the signaling lines.

The signaling paths 650, 655 and 660 may include multiplexed sets of signal lines to transfer both data and control information between the memory controller 606 and memory devices 611, 612 and 613. Alternatively, as described regarding FIG. 10, the signaling paths 650 and 660 may be employed for transferring data between the

20   memory devices 611, 612 and 613 and the memory controller 60, and signaling paths 655 may be employed for transferring timing and control information between the memory devices 611, 612 and 613 and the memory controller 603 (e.g., clock signals, read/write commands, and address information). Also, the timing information may be generated within the memory controller 606, or by external circuitry (not shown).

25   While a memory system that includes connectors for removable insertion of memory modules is depicted in FIG. 11, other system topologies may be used. As shown in FIG. 12, the memory devices 611, 612 and 613 need not be disposed on memory modules, but rather may be individually coupled to the printed circuit board 601. A connectorless interface such as that illustrated in FIG. 12 may be preferable

30   for multi-level signaling, because connectors add reflected noise and attenuation to the channels.

Alternatively, the memory devices, the memory controller and the signaling path may all be included within a single integrated circuit along with other circuitry (e.g., graphics control circuitry, digital signal processing circuitry, general purpose

processing circuitry, etc.). Such a system or that shown in FIG. 11 or FIG. 12 can be used in various electronic or optical devices, including computer systems, telephones, network devices (e.g., switch, router, interface card, etc.), handheld electronic devices and intelligent appliances.

5   Although we have focused on teaching the preferred embodiments of testing, with built-in test mechanisms, devices including a multilevel signal interfaces, other embodiments and modifications of this invention will be apparent to persons of ordinary skill in the art in view of these teachings. Therefore, this invention is limited only by the following claims, which include all such embodiments, modifications and

10   equivalents when viewed in conjunction with the above specification and accompanying drawings.

CLAIMS

1.   A device comprising:

a signal generator adapted to generate a test signals,

a transmit mechanism operably coupled to said signal generator and adapted to output a first multilevel signal based on said test signal,

a receive mechanism operably coupled to said transmit mechanism and adapted to detect a signal that crosses at least two reference levels over time, said receive mechanism outputting a detected signal based on said first multilevel signal, and

a comparison mechanism operably coupled to said receive mechanism and adapted to compare said detected signal with a reference signal, and to output an error signal if said detected signal does not match said reference signals.

2.   The device of claim 1, wherein said transmit mechanism and said receive mechanism are part of a signal interface unit.

3.   The device of claim 1, wherein said transmit mechanism is part of a first signal interface unit, said receive mechanism is part of a second signal interface unit, said first signal interface unit includes a second receive mechanism and said second signal interface unit includes a second transmit mechanism.

4.   The device of claim 3, further comprising a third interface unit having a third transmit mechanism and a third receive mechanism, wherein said third transmit mechanism is operably coupled to said second receive mechanism.

5.   The device of claim 1, wherein said transmit mechanism and said receive mechanism are connected by a bus that is affixed to a printed circuit board.

6.   The device of claim 1, wherein said transmit mechanism and said receive mechanism are contained in an integrated circuit.

7.   The device of claim 1, wherein said signal generator, said transmit mechanism, said receive mechanism and said comparison mechanism are contained in an integrated circuit.

8.   The device of claim 1, wherein said transmit mechanism is a master and said receive mechanism is a slave.

9.   The device of claim 1, wherein said receive mechanism is a master and said transmit mechanism is a slave.

10.   The device of claim 1, wherein said transmit mechanism includes a plurality of transmitters and said receive mechanism includes a plurality of receivers, with each of said transmitters being operably coupled to a corresponding one of said receivers.

11.   The device of claim 1, wherein said transmit mechanism and said receive mechanism are operably coupled to a memory.

12.   A device comprising:

        a master element including a controller and a master signal interface containing a transmit mechanism and a receive mechanism, said master being coupled to a signal pathway,

        a plurality of slave elements each including a slave signal interface containing a transmit mechanism and a receive mechanism, and being coupled to said signal pathway,

        an error detection mechanism coupled to at least one of said signal interfaces, and

        a plurality of signals communicated between said master signal interface and at least one of said slave signal interfaces over said signal pathway and checked by said error detection mechanism for errors.

13.   The device of claim 12, wherein said transmit mechanisms and said receive mechanisms each include multilevel signaling mechanisms.

14.   The device of claim 12, wherein said error detection mechanism is coupled to said one slave signal interface and said signals are sent from said master transmit mechanism to said receive mechanism of said one slave signal interface.

15.   The device of claim 12, wherein said error detection mechanism is coupled to said master signal interface and said signals are sent from said one slave transmit mechanism to said master receive mechanism.

16.   The device of claim 12, wherein said error detection mechanism is coupled to said master signal interface, said signals are sent from said master transmit mechanism to said receive mechanism of said one slave signal interface, and said signals are sent from said transmit mechanism of said one slave signal interface to said master receive mechanism.

17.   The device of claim 12, wherein said master element and said slave elements are respective integrated circuits affixed to a printed circuit board.

18.   The device of claim 12, wherein said slave elements include memory cells.

19.   A device comprising:

a base,

first, second and third conductive paths affixed to said base,

a sequence generator affixed to said base, connectable to said first conductive path and configured to generate a first sequence of signals,

a driver circuit affixed to said base and connectable to said first and second conductive paths, said driver circuit adapted to input said first sequence of signals and output onto said second conductive path a signal having a voltage level that varies in time between at least three distinct levels,

a receiver circuit affixed to said base and connectable to said second and third conductive paths, said receiver circuit adapted to receive said signal, determine which of said at least three distinct levels exists at a given time, and output onto said third conductive path a second sequence of signals, and

an error detection mechanism affixed to said base, connectable to said third conductive path and adapted to determine whether said second sequence of signals matches said first sequence of signals.

20.   The device of claim 19, wherein said driver circuit and said receiver circuit are part of a signal interface unit including an input/output pin connected to said second conductive path.

21.   The device of claim 19, wherein said driver circuit is part of a first signal interface unit, said receiver circuit is part of a second signal interface unit, said first signal interface unit includes a second receiver circuit and said second signal interface unit includes a second driver circuit.

22.   The device of claim 19, further comprising a third interface unit having a third driver circuit and a third receiver circuit, said third driver circuit connectable to said second receiver circuit by a fourth conductive path.

23.   The device of claim 19, wherein said driver circuit controls said receiver circuit.

24.   The device of claim 19, wherein said receiver circuit controls said driver circuit.

25.   A device comprising a number of signal interface units configured to communicate in parallel, said signal interface units each having a transmit mechanism and a receive mechanism, with each transmit mechanism of a first set of said signal interface units being connectable to a receive mechanism of a second set of said signal interface units.

26.   The system of claim 25, wherein said signal interface units communicate according to signals that vary in time between at least three distinct levels.

27.   A method for testing a signal interface with a test apparatus, the method comprising:

        transmitting, from the test apparatus to the signal interface, a first sequence of binary signals,

        converting, by the signal interface, said first sequence of binary signals into a sequence of multilevel signals,

        converting, by the signal interface, said sequence of multilevel signals into a second sequence of binary signals,

        comparing, by the test apparatus, said second sequence of binary signals with said first sequence of binary signals.

28.   The method of claim 27, further comprising delaying, by the test apparatus, said first sequence of binary signals for comparing with said second sequence of binary signals.

29.   The method of claim 27, further comprising selecting the signal interface from a set of signal interfaces that are coupled to each other by a plurality of switches, including providing an electrical connection between the test apparatus and the signal interface by enabling at least one of the switches.

30.   A method for testing a signal interface with a test apparatus, the method comprising:

providing a signal interface having a first set of signal interface units and a second set of signal interface units, wherein each signal interface unit of said first set is connected to one signal interface unit of said second set,

receiving, by said first set, a first sequence of binary signals,

converting, by the signal interface, said first sequence of binary signals into a sequence of multilevel signals,

transmitting, from a signal interface unit of said first to a signal interface unit of said second set, said sequence of multilevel signals,

converting, by the signal interface, said sequence of multilevel signals into a second sequence of binary signals,

comparing, by the test apparatus, said second sequence of binary signals with said first sequence of binary signals.

MSB : LSB

0 : 0 — VOUT0 = VTERM

VRH = VTERM $- (1/6)I \cdot Z_0$

0 : 1 — VOUT1 = VTERM $- (1/3)I \cdot Z_0$

VRM = VTERM $- (1/2)I \cdot Z_0$

1 : 1 — VOUT2 = VTERM $- (2/3)I \cdot Z_0$

VRL = VTERM $- (5/6)I \cdot Z_0$

1 : 0 — VOUT3 = VTERM $- I \cdot Z_0$

GROUND
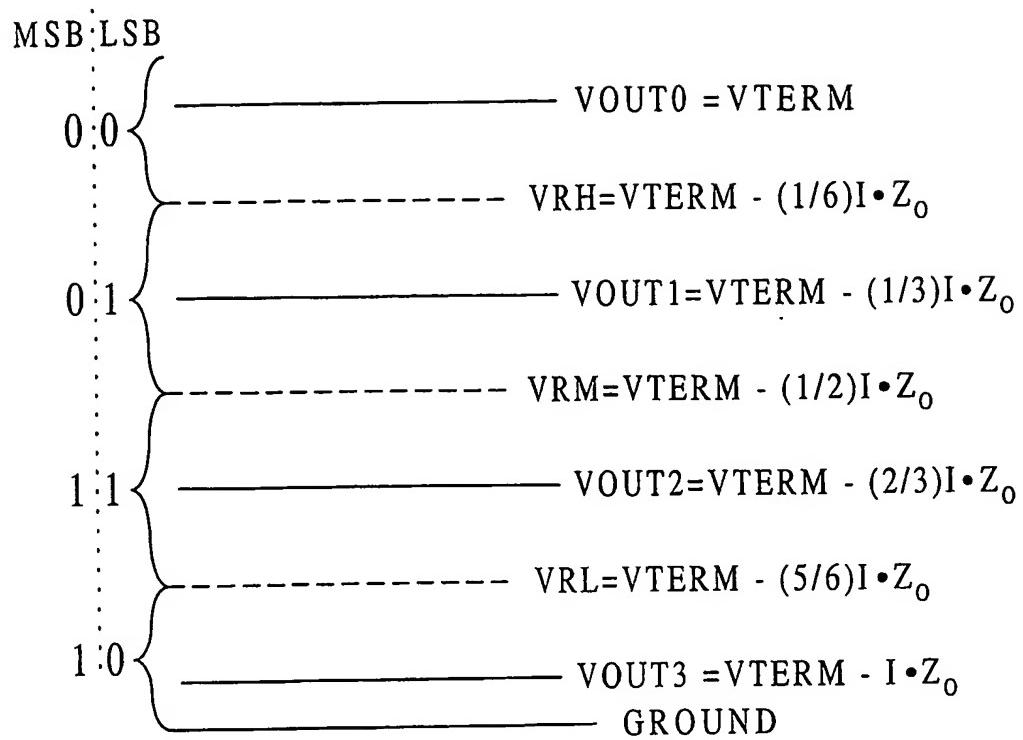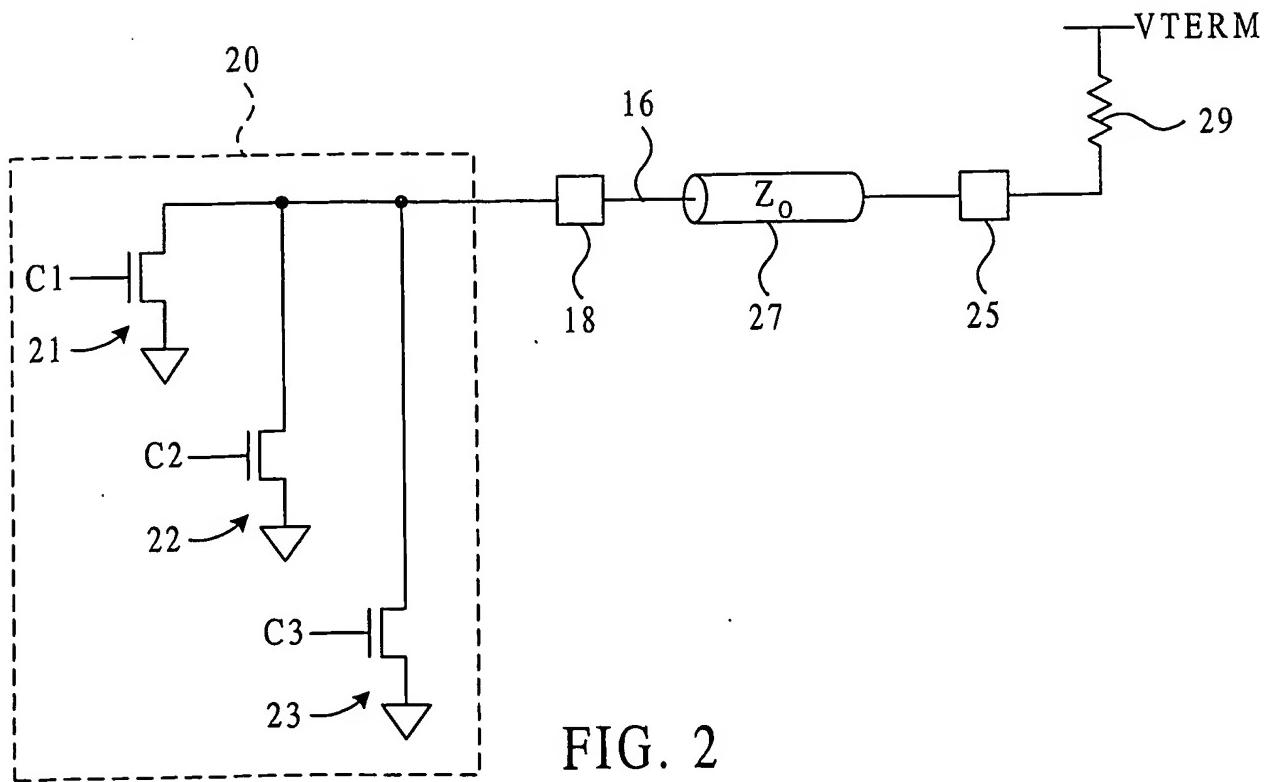
FIG. 1

FIG. 2
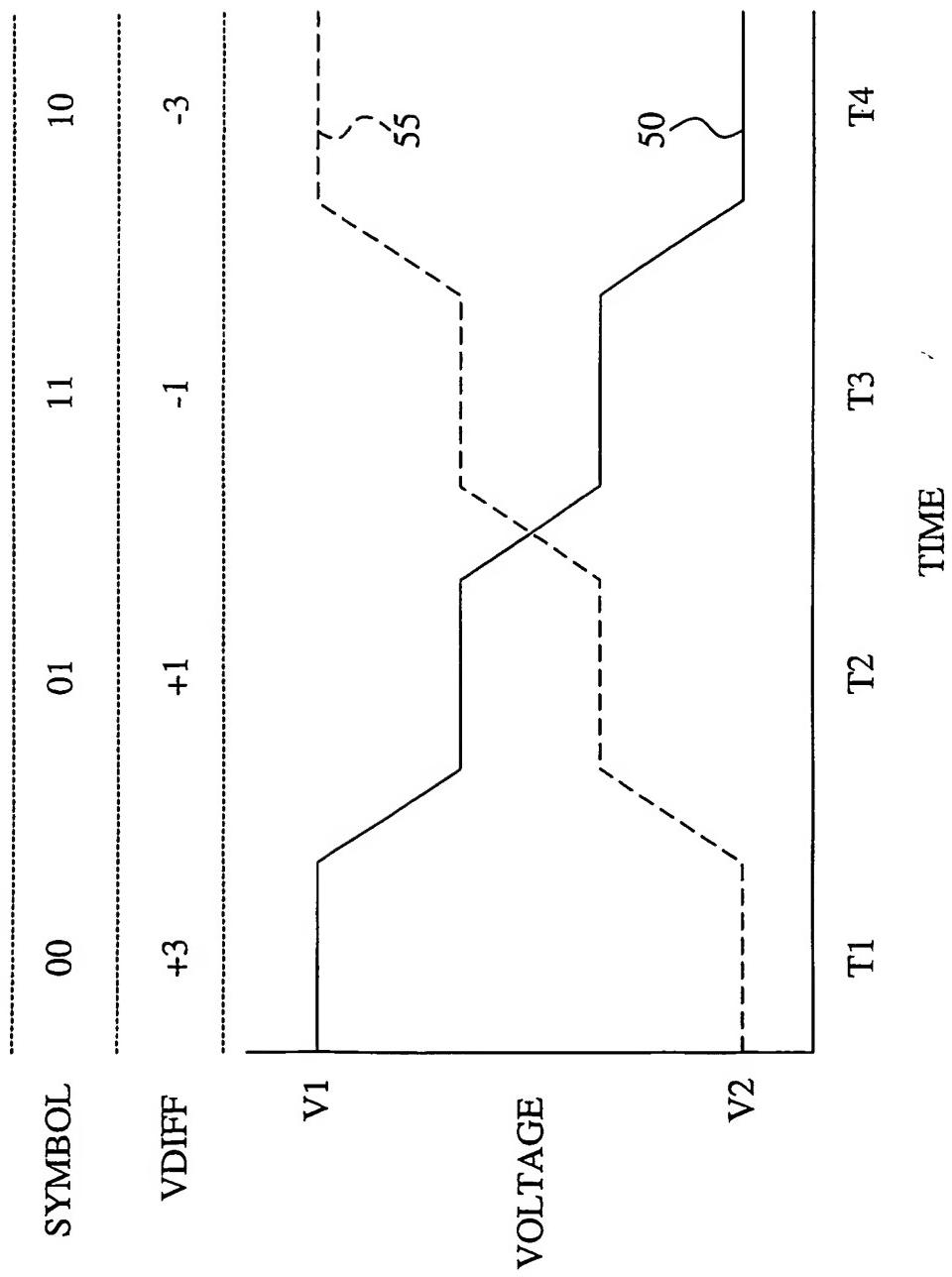
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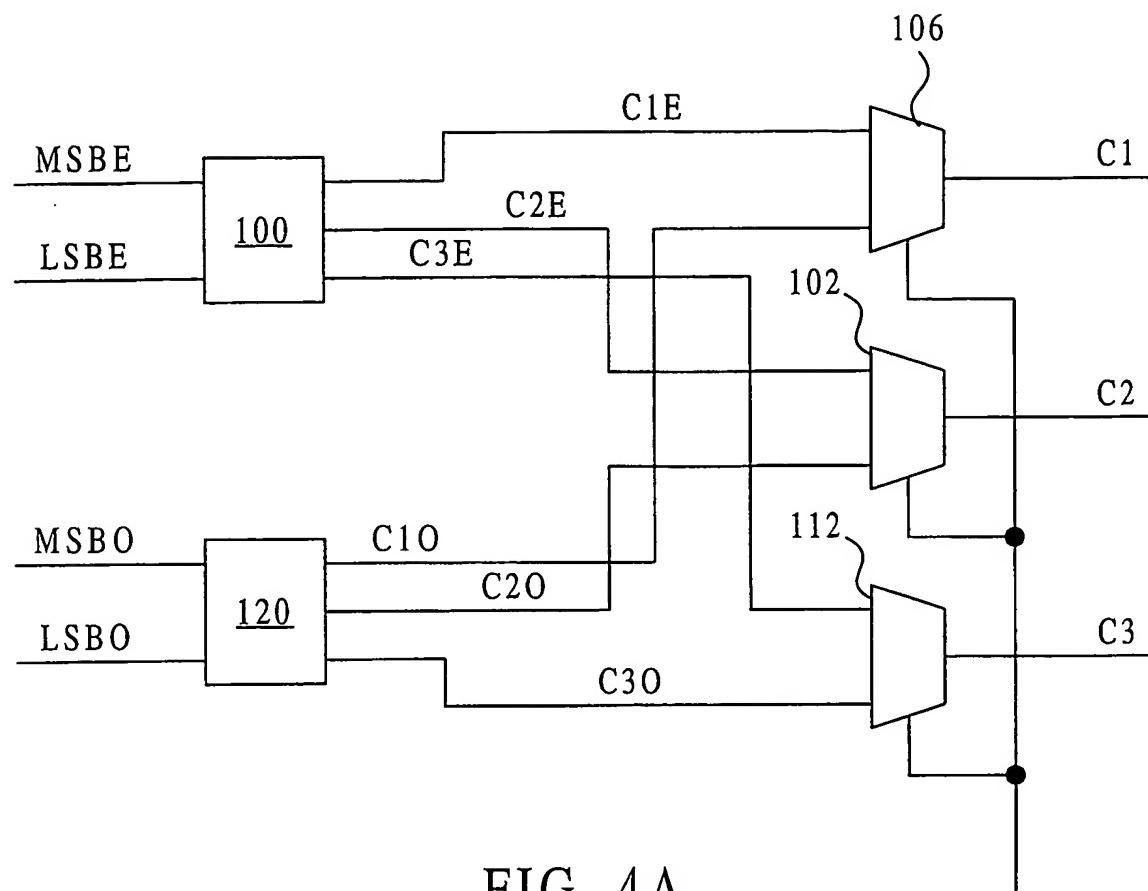
FIG. 4A
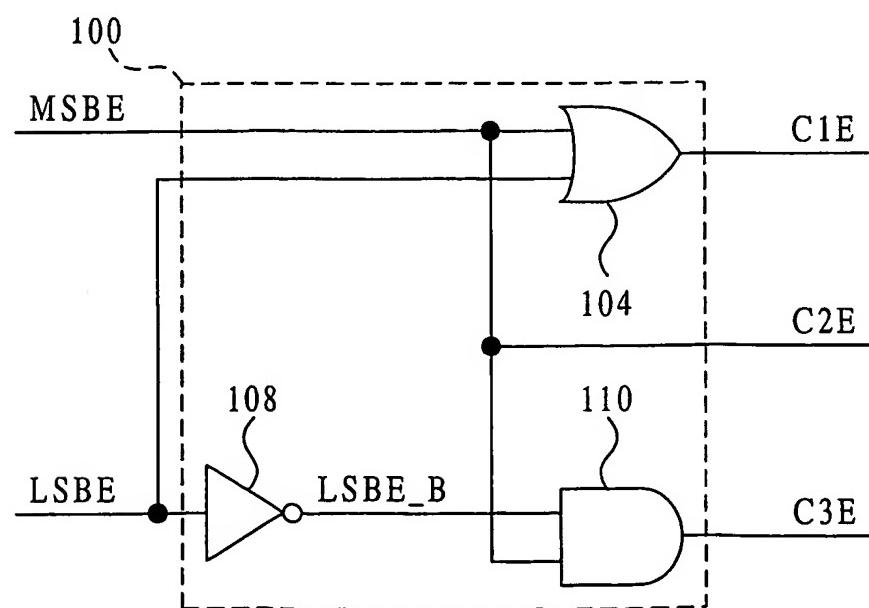
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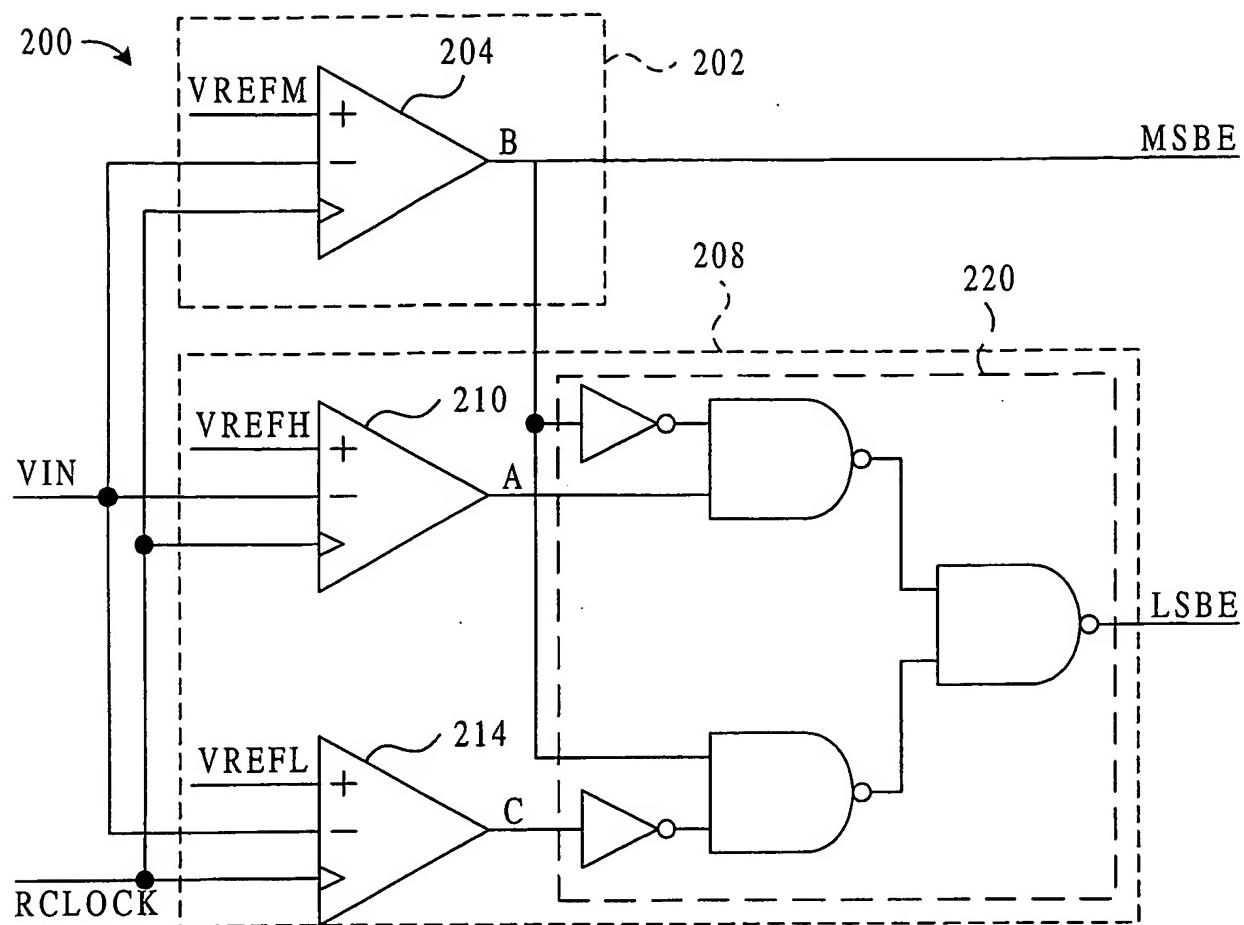
FIG. 5A

FIG. 5B

FIG. 6

FIG. 7

FIG. 8

FIG. 9A

FIG. 9B
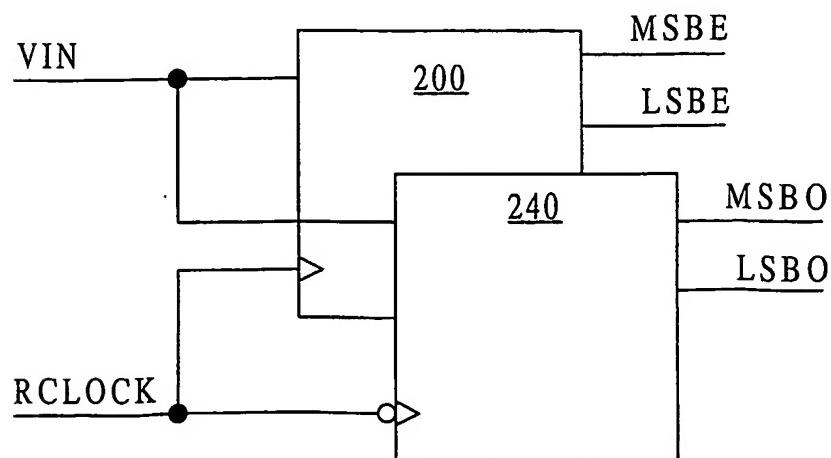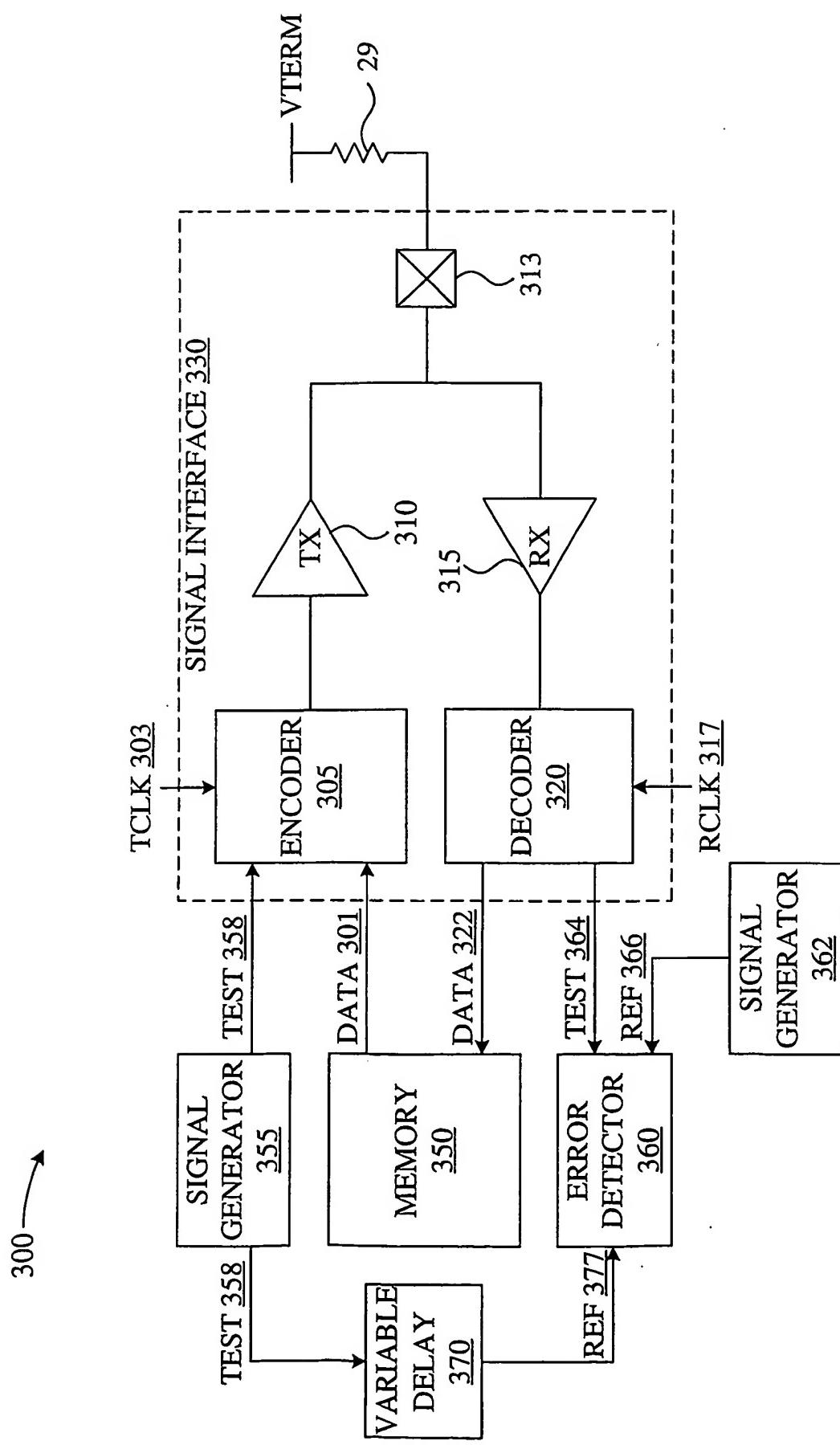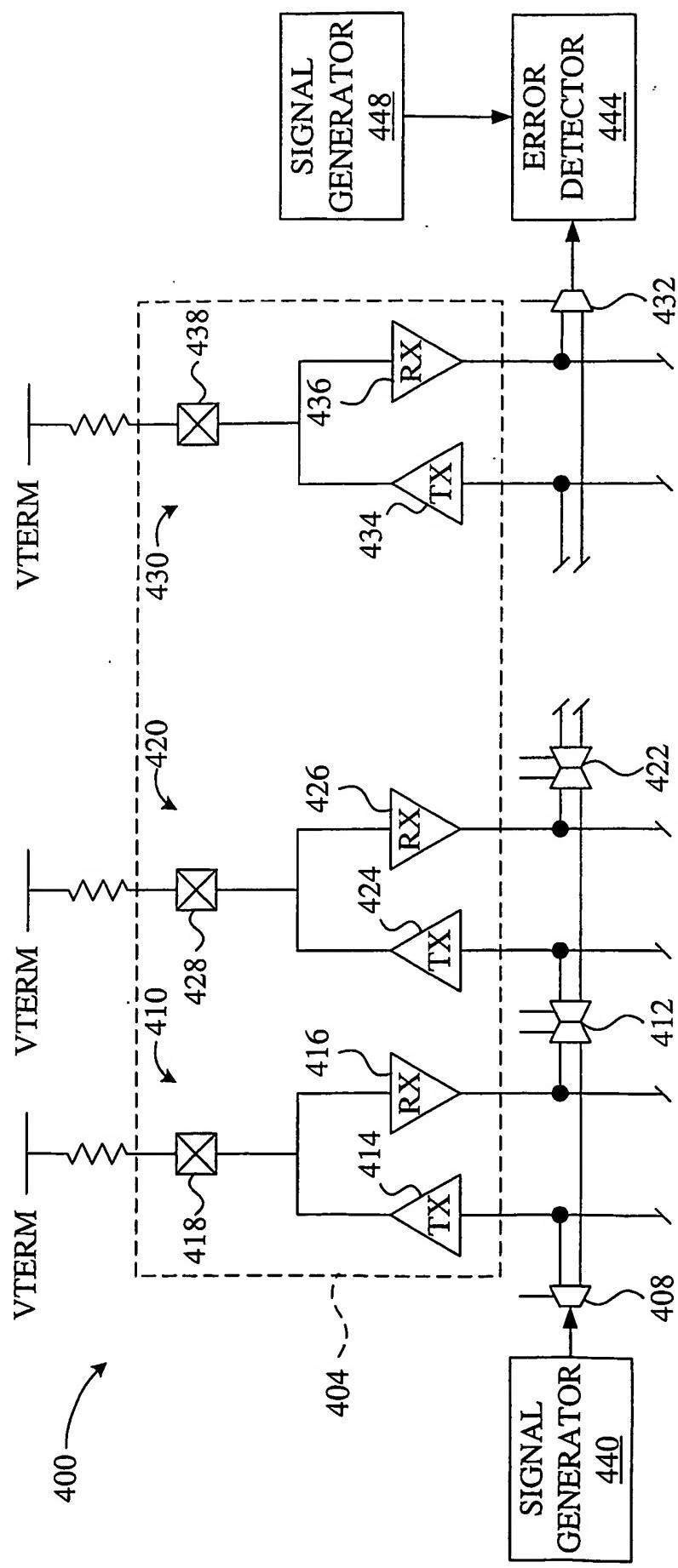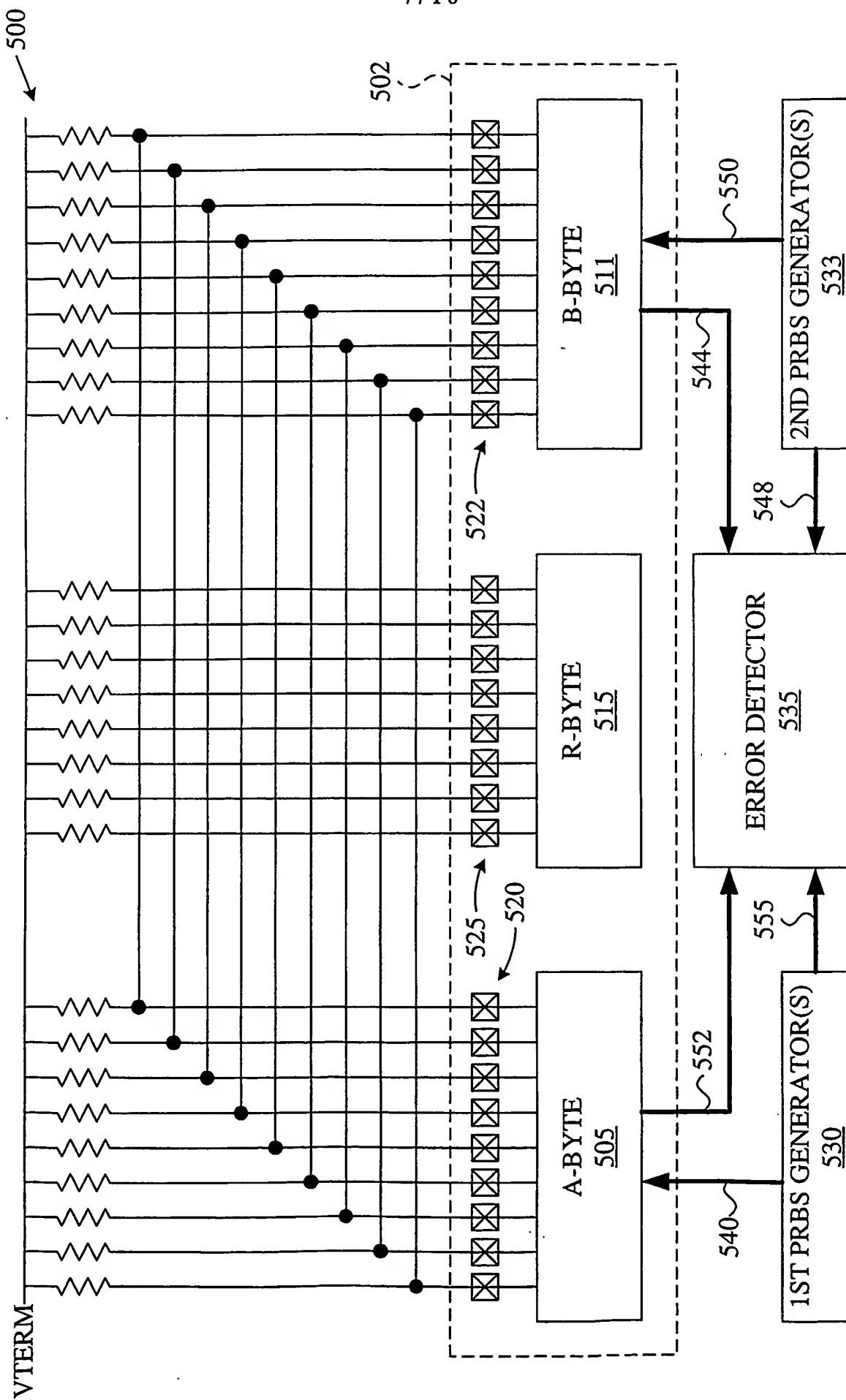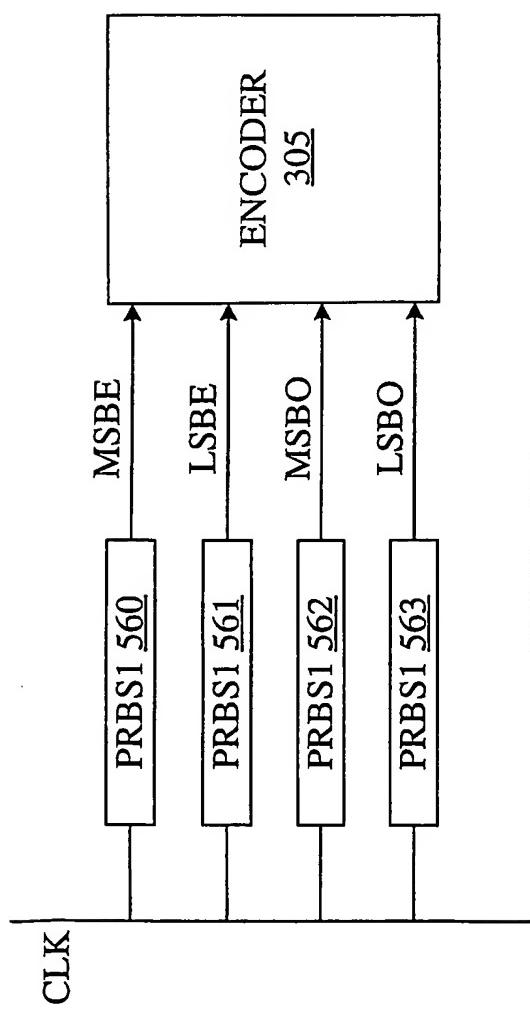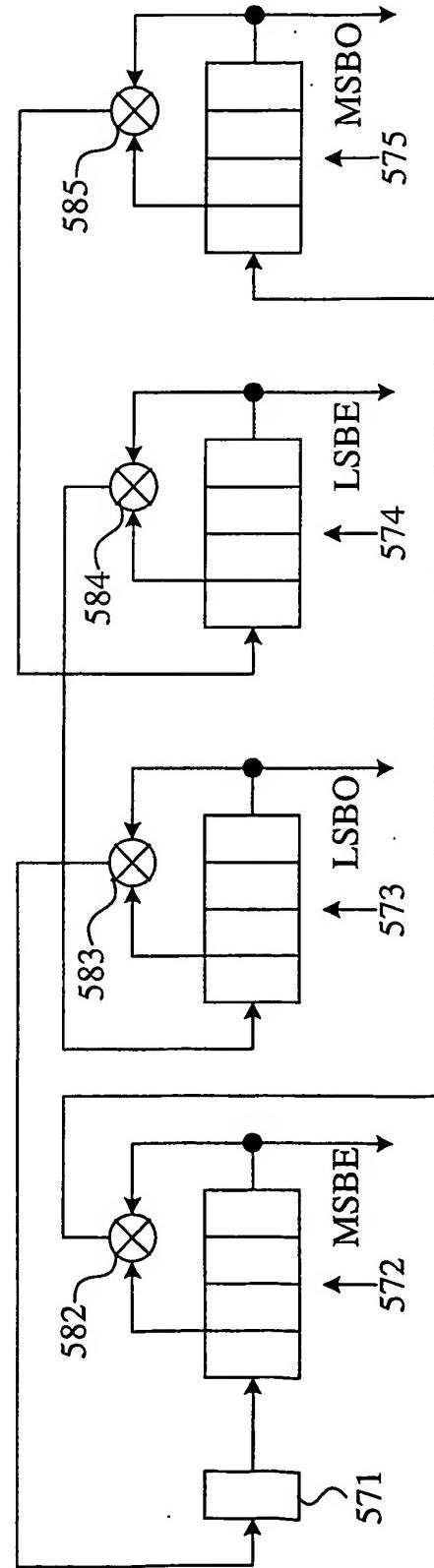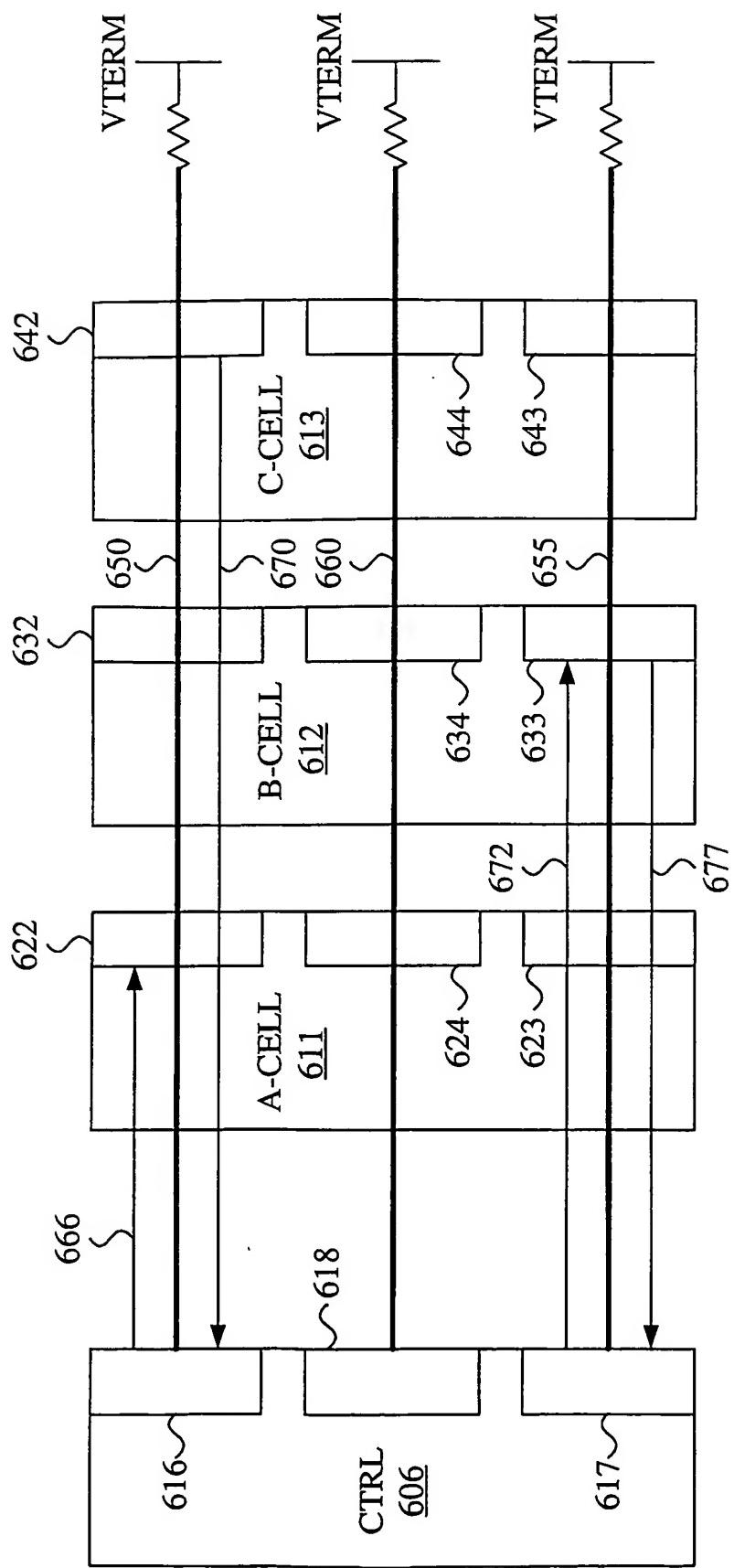
FIG. 10
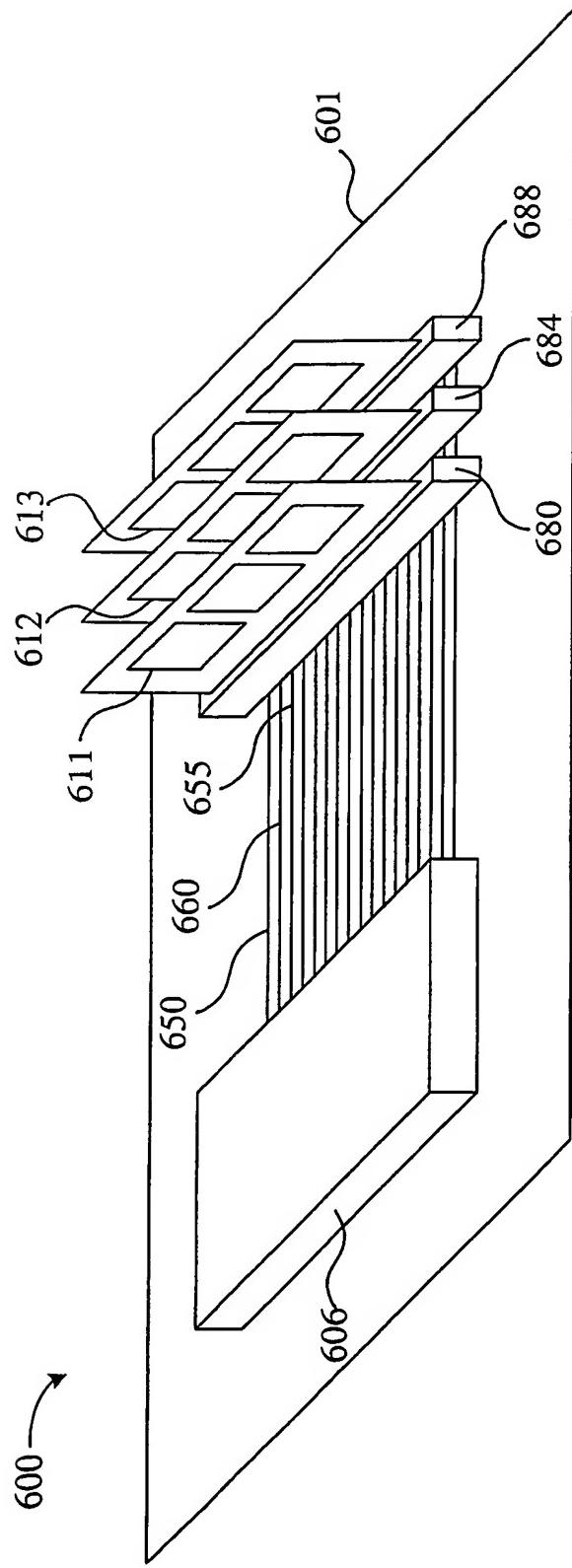
FIG. 11
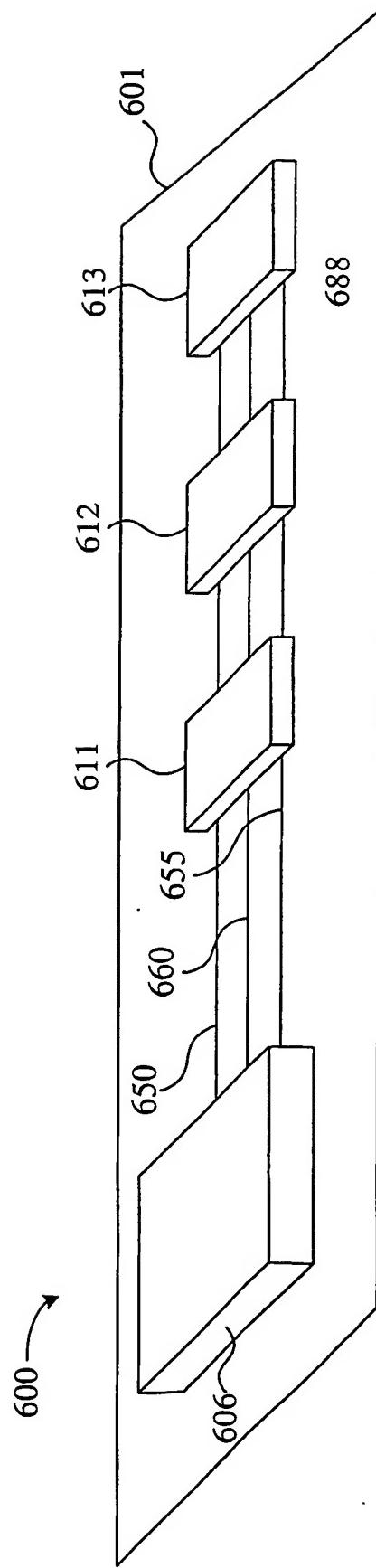
FIG. 12

INTERNATIONAL SEARCH REPORT

A.	CLASSIFICATION OF SUBJECT MATTER
IPC(7)	: GO1R 31/28; HO4B 3/46
US CL	: 714/733

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
   U.S. : 714/733, 735; 375/224

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Electronic communications systems, principles of applications of digital electronics

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
West, East, IEEE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,453,990 A (AOKI et al) 26 Sepetmber 1995 (26.09.1995), abstract, column 3, lines 7-55, claim 1.	1-30
Y	US 6,154,074 A (NAKASHIMA) 28 November 2000 (28.11.2000), abstract, column 3, lines 21-45, column 4, lines 41-59.	1-30

☐ Further documents are listed in the continuation of Box C.   ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier application or patent published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 September 2002 (27.09.2002)	0 8 NOV 2002
Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	Albert DeCady
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